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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/475,717	12/30/1999	MARK D. NARDIN	042390.P6942	6762

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EXAMINER
CRAIG, DWIN M

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 09/03/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/475,717	Applicant(s) NARDIN ET AL.	
	Examiner Dwin M Craig	Art Unit 2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12-30-1999* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 December 1999* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-17 have been presented for examination. Claims 1-17 have been examined and rejected.

Information Disclosure Statement

2. It is noted that the applicants have not provided an Information Disclosure Statement. Applicant is reminded of their duty to disclose all informational material to the patentability of the application as per 37 C.F.R. 1.56.

Drawings

3. This application has been filed with informal drawings which are acceptable for examination purposes only. Formal Drawings will be required when the application is allowed. The drawings filed on 12-30-1999 are acceptable subject to correction of the formalities listed in the attached "Notice of Draft person's Patent Drawing Review," PTO-948.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C.

122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. **Claims 1-17 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Rajgopal et al. U.S. Patent 6,363,515.** The *Rajgopal et al.* reference discloses simulating each domino circuit of a set of domino circuits **Col. 3 Lines 65-67 and Col. 4 Lines 1-22.** and reporting the results **Figure 1, Col. 7 Lines 26-39**.

As regards **Claims 1, 5, 8, 11, 14, 16 and 17** in order to simulate the circuits the simulator would have to extract parameters from the different circuits.

As regards **Claims 2** the *Rajgopal et al.* reference discloses domino logic circuit having a set of inputs and an output and simulating each domino logic circuit after any circuits coupled to the set of inputs have been simulated, **Col. 2 Lines 15-20 and Col. 3 Lines 58-65.**

As regards **Claim 3** the *Rajgopal et al.* reference discloses simulating each domino logic circuit including the simulated results of circuits coupled to the inputs of the domino logic circuit **Col. 3 Lines 58-65.**

As regards **Claims 4, 7, 8, 10, 13, 15 and 17** the *Rajgopal et al.* reference discloses a method comprising scheduling a set of domino logic circuits into an ordered list; and simulating each domino circuit according to the ordered list. **Col. 3 Lines 65-67 and Col. 4 Lines 1-22.**

As regards **Claims 6, 9 and 12** the *Rajgopal et al.* reference discloses a reporting of the results of the simulation. **Figure 1, Col. 7 Lines 26-39.**

As regards **Claim 8** the *Rajgopal et al.* reference discloses extracting parameters of non-domino circuits; further including scheduling non-domino circuits into the ordered list and simulating non-domino circuits. **Col. 4 Lines 13-67 and Col. 5 Lines 1-53.**

5. **Claims 1–17 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Heikes et al. U.S. Patent 5,798,938.** The *Heikes et al.* reference discloses simulating each domino circuit of a set of domino circuits **Col. 1 Lines 29-67 and Col. 2 Lines 1-8.** and reporting the results **Figure 8**.

As regards **Claims 4-9** the *Heikes et al.* reference discloses scheduling a set of domino logic circuits into an ordered list **Col. 2 Lines 9-40** and simulating each domino logic circuit according to the ordered list, extracting the parameters of each list, reporting the results of each simulation extracting parameters of non-domino circuits simulating the non-domino circuits and reporting the results of the non-domino circuit simulations. **Col. 3 Lines 40-61.**

As regards **Claim 10** the *Heikes et al.* reference discloses a machine readable medium embodying instructions which, when executed by a processor, cause the processor to perform a method, the method comprising: **Figure 8 and Col. 8 Lines 30-56,** scheduling a set of domino logic circuits into an ordered list; and simulating each domino logic circuit according to the ordered list. **Col. 10 Lines 55-67 and Col. 11 Lines 7-19 and Col. 12 Lines 1-16.**

As regards **Claim 11** the *Heikes et al.* reference discloses exacting the parameters for each domino logic circuit of the set of domino circuits, **Col. 2 Lines 41-67.**

As regards **Claim 12** the *Heikes et al.* reference shows **Figure 8 Item 102.**

As regards **Claim 13** the *Heikes et al.* reference discloses **Col. 2 Lines 9-40.**

As regards **Claims 14 and 17** the *Heikes et al.* reference discloses **Col. 8 Lines 31-67 and Col. 9 Lines 1-52.**

As regards **Claim 15,** see the above discussion about **Claim 10** specifically see **Col. 8 Lines 48-53** of the *Heikes et al.* reference as regards the memory controller coupled to the processor and a memory coupled to the memory controller.

As regards **Claim 16** The *Heikes et al.* reference discloses extracting the parameters for each domino circuit **Col. 4 Lines 46-67.**

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. **Claim 1** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Bosshart U.S. Patent 6,040,716** in view of **Heikes et al. U.S. Patent 5,798,938.** The *Bosshart* reference discloses a set of domino circuits being simulated. **Figures 1a, 2a, 2c, 4, 5, 6 and Col. 2 lines 35-67.** The *Bosshart* reference does not expressly disclose a method of extracting parameters of a set of domino logic circuits and reporting the results of the simulation.

The *Heikes et al.* reference discloses a method of extracting parameters of a set of domino logic circuits; **Col. 4 Lines 46-67,** and reporting the results of a simulation of the set of domino logic circuits **Figures 3-8, Col. 3 Lines 40-61.**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified *Bosshart* with *Heikes et al.* because the resulting simulation would have provided greater insight into the performance of each domino circuit in a set of domino circuits.

7. **Claims 2 and 3** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Masleid et al. U.S. Patent 5,815,687** in view of **Heikes et al. U.S. Patent 5,798,938** and in further view of **Rajgopal et al. U.S. Patent 6,363,515.** The *Masleid et al.* reference discloses simulating each domino logic circuit after any circuits coupled to the set of inputs have been simulated, **Col. 1 Lines 14-56, Figures 2, 5A, 5B and Col. 3 Lines 4-67.** The *Masleid at al.* reference does not expressly disclose extracting the parameters of a set of domino logic circuits and reporting the results of the simulation or scheduling a set of domino logic circuits into an ordered list and simulating each domino logic circuit according to the ordered list.

The *Heikes et al.* reference discloses a method of extracting parameters of a set of domino logic circuits; **Col. 3 Lines 13-31** and reporting the results of a simulation of the set of domino logic circuits, **Figures 3-8, Col. 3 Lines 40-61.**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified *Masleid et al.* with *Heikes et al.* because to perform a simulation of a circuit it is required that the parameters of that circuit be extracted and providing a report of the results is needed to assist in achieving a better design.

The *Rajgopal et al.* reference discloses scheduling a set of domino logic circuits into an ordered list and simulating each domino logic circuit according to the ordered list, **Col. 3 Lines 58-67 and Col. 4 Lines 1-7.**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified *Masleid et al.* with *Rajgopal et al.* because by simulating each domino circuit in an ordered list the simulation accurately reflects the cascading effect each preceding stage has on the stage that follows it.

The *Rajgopal et al.* reference discloses simulating each domino logic circuit including the simulated results of circuits coupled to the inputs of the domino logic circuit **Col. 3 Lines 58-67 and Col. 4 Lines 1-7.**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Masleid et al.* reference with the *Rajgopal et al.* reference because by coupling the results from earlier simulations the resulting simulation will more accurately reflect the true nature of the domino circuits.

8. **Claims 4, 5, 6, 7, 8 and 9** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Bosshart U.S. Patent 6,040,716** in view of **Heikes et al. U.S. Patent 5,798,938** and in further view of **Rajgopal et al. U.S. Patent 6,363,515.** The *Bosshart* reference discloses scheduling a set of domino logic circuits into an ordered list and simulating each domino logic circuit to the ordered list. **Col. 12 Lines 47-67 and Col. 13 Lines 1-40.** The *Bosshart* reference discloses scheduling the set of domino logic circuits such that all circuits coupled to an input of a first domino logic circuit are placed in the ordered list at a position in the ordered list before a position in the ordered list of the first domino logic circuit **Col. 12 Lines 47-67 and Col. 13 Lines 1-40.**

The *Bosshart* reference does not expressly disclose extracting the parameters for each domino circuit or reporting the results of the simulation or extracting the parameters of non-domino circuits or reporting the results of simulating the non-domino circuits.

The *Heikes et al.* reference discloses extracting the parameters for each domino circuit **Col. 3 Lines 13-31.**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Bosshart* reference with the *Heikes et al.* reference because by extracting the parameters for each domino circuit the simulation produces more accurate results.

The *Rajgopal et al.* reference discloses a reporting of the results of the simulating the domino circuits. **Figure 1, Col. 7 Lines 26-39.**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified *Bosshart* reference with *Rajgopal et al.* because reporting the results of the simulation will allow the next stage of simulation to benefit from the last simulation.

The *Rajgopal et al.* reference discloses extracting parameters of non-domino circuits; further including scheduling non-domino circuits into the ordered list and simulating non-domino circuits. **Col. 4 Lines 13-67 and Col. 5 Lines 1-53.**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified *Bosshart* with the *Rajgopal et al.* reference because being able to mix the types of logic being simulated allows for a more flexible simulation tool.

9. **Claims 10, 11, 12, 13 and 14** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Watanabe U.S. Patent 5,825,673** in view of **Rajgopal et al. U.S. Patent 6,363,515.** The

Watanabe reference discloses a machine readable medium embodying instructions which, when executed by a processor, cause the processor to perform a method, the method comprising: reporting results of the simulating. **Figure 2, item 15, Figure 3** and extracting the parameters for each non-domino logic circuit set **Figures 1, 3, 4A, 4B, 4C, 4D, 7, 8 and 9.** The *Watanabe* reference does not expressly disclose simulating each domino circuit, scheduling of the domino circuits in an ordered list such that all circuits coupled to an input of a first domino logic circuit are placed in the ordered list at a position in the ordered list before a position in the ordered list of the first domino circuit.

The *Rajgopal et al.* reference discloses scheduling the set of domino logic circuits such that all circuits coupled to an input of a first domino logic circuit are placed in the ordered list at a position in the ordered list before a position in the ordered list of the first domino logic circuit, **Col. 4 Lines 13-22.**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Watanabe* reference with the *Rajgopal et al.* reference because by placing the domino circuits in an ordered list the simulation will more accurately reflect the real performance of the multiple domino circuits due to the dependence of each succeeding logic circuit stage on the output parameters of the preceding logic circuit stage.

10. **Claims 15 and 16** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Watanabe U.S. Patent 5,825,673** in view of in view of **Rajgopal et al. U.S. Patent 6,363,515.** The *Watanabe* reference discloses a processor; a memory controller; a memory coupled to a memory controller; **Figure 2 and Col. 4 Lines 31-57,** wherein the processor executes

instructions to perform a method, the method comprising: reporting results of the simulating. **Figure 2, item 15, Figure 3** and extracting the parameters for each non-domino logic circuit set **Figures 1, 3, 4A, 4B, 4C, 4D, 7, 8 and 9.** The *Watanabe* reference does not expressly disclose simulating each domino circuit, scheduling of the domino circuits in an ordered list such that all circuits coupled to an input of a first domino logic circuit are placed in the ordered list at a position in the ordered list before a position in the ordered list of the first domino circuit.

The *Rajgopal et al.* reference discloses scheduling the set of domino logic circuits such that all circuits coupled to an input of a first domino logic circuit are placed in the ordered list at a position in the ordered list before a position in the ordered list of the first domino logic circuit, **Col. 4 Lines 13-22.**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Watanabe* reference with the *Rajgopal et al.* reference because by placing the domino circuits in an ordered list the simulation will more accurately reflect the real performance of the multiple domino circuits due to the dependence of each succeeding logic circuit stage on the output parameters of the preceding logic circuit stage.

11. **Claim 17** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Masleid et al. U.S. Patent 5,815,687** in view of **Heikes et al. U.S. Patent 5,798,938** and in further view of **Rajgopal et al. U.S. Patent 6,363,515.** The *Masleid et al.* reference discloses an apparatus comprising for a set of domino logic circuits **Figures 1, 2, 5A, 5B and Col. 1 Lines 15-57.**

The *Masleid et al.* reference does not expressly disclose a means for extracting parameters for each domino circuit of a set of domino circuits.

The *Heikes et al.* reference discloses extracting the parameters for each domino circuit **Col. 4 Lines 46-67.**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Masleid et al.* reference with the *Heikes et al.* because extracting parameters from each domino circuit provides for a better simulation.

The *Masleid et al.* reference does not expressly disclose a means for scheduling the set of domino circuits into an ordered list or a means for simulating the domino circuits according to that ordered list.

The *Rajgopal et al.* reference discloses a method comprising scheduling a set of domino logic circuits into an ordered list; and simulating each domino circuit according to the ordered list. **Col. 3 Lines 65-67 and Col. 4 Lines 1-22.**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Masleid et al.* reference with the *Rajgopal et al.* reference because each stage that is simulated needs the output data from the previous stage in order to properly simulate the current condition of that stage of the domino circuit.

The *Masleid et al.* reference does not expressly disclose a means for reporting results of the means for simulating.

The *Rajgopal et al.* reference discloses a reporting of the results of the simulation, **Figure 1, Col. 7 Lines 26-39.**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Masleid et al.* reference with the *Rajgopal et al.* reference because reporting

the result of the simulation provides the user of the simulation the information needed for better domino circuit design.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dwin M Craig whose telephone number is 703 305-7150. The examiner can normally be reached on 9:00 - 5:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on 703 305-9704. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 305-3900.

DMC
August 24, 2002

William Thomson
A.U. 2123

Attachment for PTO-948 (Rev. 03/01, or earlier)
6/18/01

The below text replaces the pre-printed text under the heading, "Information on How to Effect Drawing Changes," on the back of the PTO-948 (Rev. 03/01, or earlier) form.

INFORMATION ON HOW TO EFFECT DRAWING CHANGES

1. Correction of Informalities -- 37 CFR 1.85

New corrected drawings must be filed with the changes incorporated therein Identifying indicia, if provided, should include the title of the invention, inventor's name, and application number, or docket number (if any) if an application number has not been assigned to the application. If this information is provided, it must be placed on the front of each sheet and centered within the top margin. If corrected drawings are required in a Notice of Allowability (PTOL-37), the new drawings **MUST** be filed within the **THREE MONTH** shortened statutory period set for reply in the Notice of Allowability. Extensions of time may NOT be obtained under the provisions of 37 CFR 1.136(a) or (b) for filing the corrected drawings after the mailing of a Notice of Allowability. The drawings should be filed as a separate paper with a transmittal letter addressed to the Official Draftsperson.

2. Corrections other than Informalities Noted by Draftsperson on form PTO-948.

All changes to the drawings, other than informalities noted by the Draftsperson, **MUST** be made in the same manner as above except that, normally, a highlighted (preferably red ink) sketch of the changes to be incorporated into the new drawings **MUST** be approved by the examiner before the application will be allowed. No changes will be permitted to be made, other than correction of informalities, unless the examiner has approved the proposed changes

Timing of Corrections

Applicant is required to submit the drawing corrections within the time period set in the attached Office communication. See 37 CFR 1.85(a).

Failure to take corrective action within the set period will result in ABANDONMENT of the application

Attachment 09/475,719

The drawings submitted with this application were declared informal by the applicant. Accordingly they have not been reviewed by a draftsperson at this time. When formal drawings are submitted, the draftsperson will perform a review.

Direct any inquires concerning drawing review to the Drawing Review Branch (703) 305-8404.